

IFIN

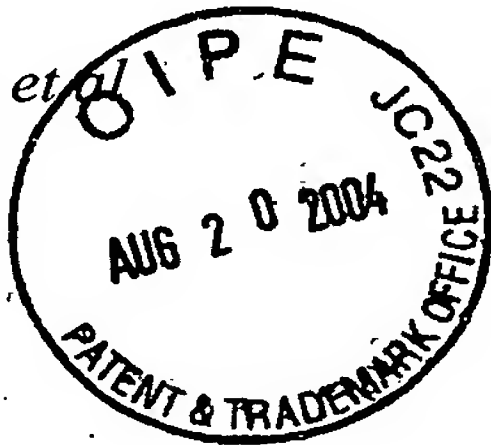
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: SAHA *et al.*

Appl. No.: 10/710861

Filed: August 09, 2004

For: Providing Optimal Supply Voltage to Integrated Circuits



Art Unit: UNASSIGNED

Examiner: UNASSIGNED

Atty. Docket: TI-36220

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Listed below on an attached Form PTO-1449 is information known to applicant(s). A copy of each listed publication and foreign patent is being submitted herewith, along with a concise explanation of information in a foreign language, if any, pursuant to 37 C.F.R. §1.97-1.98.

Applicants respectfully request that the listed information be considered by the Examiner and be made of record in the above-identified application. The Examiner is requested to initial and return it in accordance with MPEP §609.

This statement is not intended to represent that the information cited in the statement is, or is considered to be, material to patentability as defined in §1.56. Applicant reserves the right to establish patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information is not enabling for the teachings purportedly offered.

X This statement qualifies under 37 C.F.R. §1.97, subsection (b) because (check all that apply):

- X (1) It is being filed within 3 months of the application filing date; OR
— (2) It is being filed within 3 months of entry of a national stage; OR
X (3) It is being filed before the mail date of the first Office Action on the merits.

— 37 C.F.R. §1.97(c). If this statement is being filed after the latest of: (1) three months beyond the filing date of a national application; (2) three months beyond the date of entry of the national stage as set forth in §1.491 in an international application; or (3) the mailing date of a first Office action on the merits, but before the mailing date of the earlier of a final office action under §1.113 or a notice of allowance under §1.311, then:
— a certification as specified in §1.97(e) is provided below; **or**
— a fee of \$180.00 as set forth in §1.17(p) is authorized below, enclosed, or included with the payment of other papers filed together with this statement.

— 37 C.F.R. §1.97(d). If this statement is being filed after the mailing date of the earlier of a final office action under §1.113 or a notice of allowance under §1.311, but before payment of the issue fee, then:
A. a certification as specified in §1.97(e) is submitted herewith; **and**
B. a petition under 37 C.F.R. §1.97(d) requesting consideration of this statement is submitted herewith; **and**
C. a fee of \$130.00 as set forth in §1.17(i)(1) is authorized below, enclosed, or included with the payment of other papers filed together with this statement.

Respectfully submitted,

Date: August 10, 2004

By: Naren Thappeta
Narendra Reddy Thappeta
Registration Number: 41,416

Law Firm of Naren Thappeta
Phone/Fax: + 1 (707) 356-4172
Email: nt@iphorizons.com

U.S. PATENT DOCUMENTS

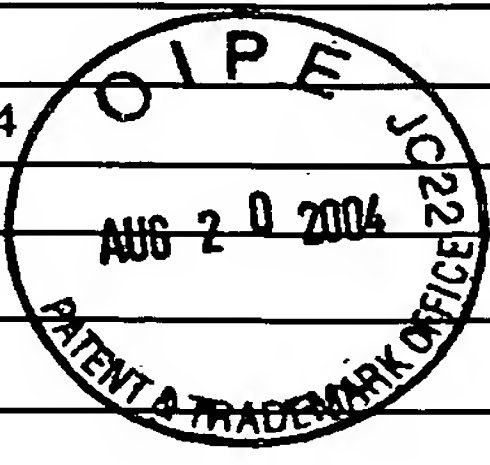
FOREIGN PATENT DOCUMENTS

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.**

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if Known	
				Application Number	10/710,861
				Filing Date	August 09, 2004
				First Named Inventor	Anindya SAHA
				Group Art Unit	UNASSIGNED
				Examiner Name	UNASSIGNED
Sheet	2	of	2	Attorney Docket Number	TI-36220



OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	$\frac{1}{2}$
		PETER MACKEN, MARC DEGRAUWE, MARK VAN PAEMEL, HENRI OGUEY, "A Voltage Reduction Technique for Digital Systems" in ISSCC 90/ Session 15. Innovative Circuit design, Swiss Center for Electronics and Microtechnology (CSEM) Neuchel Switzerland/ FPM 15.2, pp.238 - 239/ Friday, February 16, 1990	
		THOMAS D. BURD AND ROBERT W BRODERSEN, "Design Issues for Dynamic Voltage Scaling", ISLPED '00 Rapallo, Italy, Berkeley Wireless Research center, University of California, CA/ pp.09 - 14, ACM, 2000	
		THOMAS BURD, TROVOR PERING, ANTHONY STRATAKOS AND ROBERT BRODERSEN, "A Dynamic Voltage Sealed Microprocessor System". ISSCC 2000/Session 17/ Logic and Systems/Paper WA 17.4, Berkeley Wireless Research center, University of California, CA, pp.294 - 295, 466, IEEE 2000	
		TAJANA SIMUNIC, LUCA BENINI, ANDREA ACQUAVIVA, PETER GLYNN AND GIOVANNI DE MICHELI. "Dynamic Voltage Scaling and Power Management for Portable Systems", pp. 524 - 529, Las Vegas, Nevada, USA, DAC 2001, June 18-22, 2001	
		KEVIN J. NOWKA, GARY D. CARPENTER, ERIC W. MAC DONALD, HUNG C. NGO, BISHOP C. BROCK, KOJI I. ISHII, TUYET Y. NGUYEN AND JEFFREY L. BURNS. "A 32-bit PowerPC System-on-a-Chip with support for Dynamic Voltage Scaling and Dynamic Frequency Scaling", in IEEE Journal of Solid State Circuits Vol.37, pp.1441 - 1447, NO.11 November 2002.	
		REX MIN, TRAVIS FURRER AND ANANTHA CHANDRAKASAN, "Dynamic Voltage Scaling Techniques for Distributed Microsensor Networks", Department of EECS, Massachusetts Institute of Technology. 2002	
		MOHAMED ELGEBALY, AMR FAHIM, INYUP KANG AND MANOJ SACHDEV, "Robust and Efficient Dynamic Voltage Scaling Architecture" Department of Electrical and Computer Engineering, University of Waterloo, Ontario, N2L 3G1 Canada, Qualcomm Inc, San Diego, CA, 92121 USA. IN IEEE, PP. 155- 158, 2003.	
		A.SOTO. A DE CASTRO, P. ALOU, J.A. CAO BOS, J. UCEDA AND A. LOTFI. "Analysis of the Buck Converter for Scaling the Supply Voltage of Digital Circuits". Universidad Politecnica de Madrid (UPM), Spain and Enpirion Inc, USA, IN IEEE, PP. 711 - 717, 2003	

Examiner Signature		Date Considered	
-----------------------	--	--------------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.